REMARKS

The Official Action mailed December 11, 2007, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on September 20, 2006; and December 12, 2006.

Claims 1-13 were pending in the present application prior to the above amendment. Claims 1-11 and 13 have been amended to better recite the features of the present invention, and new dependent claims 14-28 have been added to recite additional protection to which the Applicant is entitled. The Applicant notes with appreciation the indication of the allowability of dependent claim 7 (page 5, Paper No. 20071128). Accordingly, claims 1-28 are now pending in the present application, of which claims 1-6, 10 and 11 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

The Official Action objects to the abstract asserting that "it does not contain a single paragraph within a separate sheet as required" (page 2, Id.). In response, the Applicant has amended the Abstract on a separate sheet as shown in the attached replacement sheet. Accordingly, reconsideration and withdrawal of the objection are in order and respectfully requested.

In response to a request in the Official Action, the Applicant will correct any errors in the specification of which the Applicant becomes aware.

The Official Action rejects claims 7, 8 and 13 under 35 U.S.C. § 112, second paragraph. Specifically, regarding claim 7, the Official Action asserts that "the recitation 'the amount' on line 2 lacks clear antecedent basis" and that "[i]t is not understood how the terminal on line 2 can control the amount of charge when it is not connected to anything and the terminal is not a control circuit to perform the control function, and

where the terminal comes from" (page 2, Id.). Also, regarding claims 8 and 13, the Official Aciton asserts that "the description of the present invention is incomplete because the 'resistor' is not connected to anything" (page 3, Id.).

In response, the Applicant has amended claims 7, 8 and 13 so that the claims are definite. Dependent claim 7 was previously a multiple dependent claim. Claim 7 has been amended to depend from claim 1, new dependent claims 14-18 have been added, which are based on claim 7 and which depend from independent claims 2-6, respectively. Claims 7 and 14-18 recite a connection of the connecting terminal. Specifically, claim 7 recites that the connecting terminal is connected to the drain of the transistor; claim 14 recites that the connecting terminal is connected to the source of the transistor; claim 15 recites that the connecting terminal is connected to the drain of the one of the plurality of transistors; claim 16 recites that the connecting terminal is connected to the source of the one of the plurality of transistors; claim 17 recites that the connecting terminal is connected to the drain of the second transistor; and claim 18 recites that the connecting terminal is connected to the source of the second transistor. These features are supported in the present specification, for example, by page 11, lines 23-26.

Dependent claim 8 was previously a multiple dependent claim. Claim 8 has been amended to depend from claim 1, and new dependent claims 19-23 have been added, which are based on claim 8 and which depend from independent claims 2-6, respectively. Claims 8 and 19-23 recite a connection of the resistor. Specifically, claim 8 recites that the drain of the transistor is connected to the input terminal through the resistor; claim 19 recites that the source of the transistor is connected to the input terminal through the resistor; claim 20 recites that the drain of the one of the plurality of transistors is connected to the input terminal through the resistor; claim 21 recites that the source of the one of the plurality of transistors is connected to the input terminal through the resistor; claim 22 recites that the drain of the second transistor is connected to the input terminal through the resistor; and claim 23 recites that the source of the

second transistor is connected to the input through the resistor. These features are supported in the present specification, for example, by page 8, lines 7-15.

With respect to rejection of claim 13, claims 10 and 11 have been amended to recite that the drain and the control gate are connected to an input terminal and an output terminal, and claim 13 has been amended to recite that the drain of the transistor is connected to the input terminal through the resistor. These features are also supported in the present specification, for example, by page 8, line 7-15.

The Applicant respectfully submits that amended claims 7, 8 and 13 are definite. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 112 are in order and respectfully requested.

The Official Action rejects claims 1, 2, 8 and 9 as anticipated by U.S. Patent No. 6,670,679 to Hirata. The Applicant respectfully submits that an anticipation rejection cannot be maintained against the independent claims of the present application, as amended. The Official Action rejects claims 3-6 and 10-13 as obvious based on U.S. Patent No. 6,670,679 to Hirata. The Applicant respectfully submits that a *prima facie* case of obviousness cannot be maintained against the independent claims of the present application, as amended.

As stated in MPEP § 2131, to establish an anticipation rejection, each and every element as set forth in the claim must be described either expressly or inherently in a single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some reason, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the

prior art to produce the claimed invention where there is some reason to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach, either explicitly or inherently, or suggest all the features of the independent claims, as amended. Independent claims 1-6, 10 and 11 have been amended to recite that a floating gate is formed over a semiconductor layer with a first insulating film interposed therebetween, the floating gate and a control gate overlap each other with a second insulating film interposed therebetween, a side surface of the floating gate is covered with a third insulating film, and the floating gate is insulated from the semiconductor layer. These features are supported in the present specification, for example, by Embodiment 5 and Figure 11B. Hirata appears to teach "a floating gate connected to a source line or a ground line (column 4, lines 15-24). However, Hirata does not teach, either explicitly or inherently, or suggest that a floating gate is formed over a semiconductor layer with a first insulating film interposed therebetween, the floating gate and a control gate overlap each other with a second insulating film interposed therebetween, a side surface of the floating gate is covered with a third insulating film, and the floating gate is insulated from the semiconductor layer.

Since Hirata does not teach, either explicitly or inherently, or suggest the above-referenced features of the present invention, anticipation and obviousness rejections cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. §§ 102 and 103 are in order and respectfully requested.

New claims 14-28 have been added to recite additional protection to which the Applicant is entitled. At this opportunity, the Applicant has amended claim 9. Dependent claim 9 was previously a multiple dependent claim. Claim 9 has been amended to depend from claim 1, and new dependent claims 24-28 have been added, which are based on claim 9 and which depend from independent claims 2-6, respectively. The features of claims 14-28 are supported in the present specification as noted above. For the reasons stated above, the Applicant respectfully submits that new claims 14-28 are in condition for allowance.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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